AN10741

TDF8597, TDF8599A and TDF8599B class-D automotive amplifiers

Rev. 1 — 18 November 2011 **Application note**

Document information

Info	Content
Keywords	TDF8597TH (6 V to 24 V), TDF8599ATH (35 V), TDF8599BTH (24 V) Class-D, audio, amplifier, stereo BTL, automotive, diagnostics
Abstract	The TDF8597 and TDF8599A and B are stereo BTL class-D amplifiers designed for automotive applications. They are capable of driving 2 Ω loads in stereo mode (TDF8597 and TDF8599B) and 1 Ω loads in parallel mode. Variants with supply voltage ranges of 6 V, 24 V and 35 V make them suitable for use in head-units and in high power multi-channel audio systems.

Revision history

Rev	Date	Description
v.1	20111118	initial version

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1. Introduction

The TDF8597, TDF8599A and TDF8599B are stereo BTL class-D amplifiers, designed for use in automotive applications.

Some application information is provided in the individual device data sheets, however this application note describes the available application PCB and the I²C-bus control software.

Some general information is provided for quick reference.

1.1 General description

The TDF8597, TDF8599B and TDF8599A are dual bridge-tied load (BTL) car audio amplifiers each comprising an NDMOST-NDMOST output stage based on SOI BCDMOS technology. The amplifiers can be controlled with or without I²C. With I²C control, DC load detection results and fault conditions can be read.

The TDF8597, TDF8599A and TDF8599B are high efficiency class-D amplifiers with low dissipation. Due to the low dissipation, the devices can be used with a much smaller heat sink than standard class-AB amplifiers. The TDF8597 fully supports start/stop systems as it can operate at a battery voltage as low as 6 V.

The TDF8599A can operate up to supply voltages of 35V, making it very suitable for high power audio systems.

The TDF8597 has six possible I²C addresses selected by external resistor values connected to pins ADS and MOD. If pin ADS is shorted to ground, the TDF8597 operates in non-I²C mode, and no I²C-bus communication is possible. Operating and mute modes can only be selected using pins EN and ON.

The TDF8599A and TDF8599B offer 15 I²C-bus addresses and, like the TDF8597, can also be used in non-I²C mode.

All devices are pin-to-pin compatible.

1.2 Quick reference data

Table 1. Quick reference data: TDF8597

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General; V_P = 14.4 V						
V_P	supply voltage		6	14.4	24	V
I_P	supply current	off state; V_{EN} < 0.8 V	-	2	10	μA
I_q	quiescent current	no load, snubbers and output filter connected	-	90	120	mA
Stereo mode; V_P = 14.4 V						
P_o	output power	R_L = 4 Ω; THD = 10 %	24	26	-	W
		R_L = 2 Ω; THD = 10 %	39	43	-	W
Stereo mode; V_P = 24 V						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	70	-	W
		R_L = 2 Ω; THD = 10 %	-	100	-	W

Table 1. Quick reference data: TDF8597 *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Parallel mode; V_P = 14.4 V						
P_o	output power	R_L = 1 Ω; THD = 10 %	-	85	-	W
Parallel mode; V_P = 24 V						
P_o	output power	R_L = 2 Ω; THD = 10 %	-	138	-	W
		R_L = 1 Ω; THD = 1 %	135	150	-	W

Table 2. Quick reference data: TDF8599B

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General; V_P = 14.4 V						
V_P	supply voltage		8	14.4	24	V
I_P	supply current	off state; V_{EN} < 0.8 V	-	2	10	μA
I_q	quiescent current	no load, snubbers and output filter connected	-	90	120	mA
Stereo mode; V_P = 14.4 V						
P_o	output power	R_L = 4 Ω; THD = 10 %	24	26	-	W
		R_L = 2 Ω; THD = 10 %	39	43	-	W
Stereo mode; V_P = 24 V						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	70	-	W
		R_L = 2 Ω; THD = 10 %	-	100	-	W
Parallel mode; V_P = 14.4 V						
P_o	output power	R_L = 1 Ω; THD = 10 %	-	85	-	W
Parallel mode; V_P = 24 V						
P_o	output power	R_L = 2 Ω; THD = 10 %	-	138	-	W
		R_L = 1 Ω; THD = 1 %	135	150	-	W

Table 3. Quick reference data: TDF8599A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General; V_P = 14.4 V						
V_P	supply voltage		8	14.4	35	V
I_P	supply current	off state; V_{EN} < 0.8 V	-	2	10	μA
I_q	quiescent current	no load, snubbers and output filter connected	-	90	120	mA
Stereo mode; V_P = 14.4 V						
P_o	output power	R_L = 4 Ω; THD = 10 %	23	25	-	W
		R_L = 2 Ω; THD = 10 %	34	38	-	W
Stereo mode; V_P = 35 V						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	135	-	W
Parallel mode; V_P = 14.4 V						
P_o	output power	R_L = 2 Ω; THD = 10 %	-	50	-	W
Parallel mode; V_P = 35 V						
P_o	output power	R_L = 2 Ω; THD = 10 %	-	250	-	W

1.3 Main differences between devices

The main differences between the TDF8597, TDF8599A and TDF8599B are shown in Table 4.

Table 4. Differences between the TDF8597, TDF8599B and TDF8599A

Parameter	TDF8597	TDF8599B	TDF8599A
Minimum supply voltage ($V_{P(min)}$)	6 V	8 V	8 V
Maximum supply voltage ($V_{P(max)}$)	24 V	24 V	35 V
Minimum load resistance ($R_{L(min)}$) stereo mode	2 Ω	2 Ω	4 Ω
Minimum load resistance ($R_{L(min)}$) parallel mode	1 Ω	1 Ω	2 Ω
Total harmonic distortion clip detection level (THD_{clip})	0.2 %/10 % selectable	0.2 %	0.2 %
Short-circuit across load detection at start-up	yes	only with workaround [1]	only with workaround [1]
Number of I^2C addresses possible	6	15	15

[1] See Section 4.2.

Table 4 shows that the TDF8597 and the TDF8599B are similar. The TDF8597, however, can operate with a supply voltage as low as 6 V, detects short-circuits across the load at start-up and has two selectable clip diagnostic levels. The only restriction that the TDF8597 has compared to the TDF8599B, is that it only has 6 selectable I^2C addresses.

The TDF8599A can operate with a supply voltage as high as 35 V, enabling it to deliver up to 135 W per channel into 4 Ω loads. The output transistors of the TDF8599A have a slightly higher R_{DSon} than those in the TDF8597 and the TDF8599B. Therefore, the output power at a supply voltage of 14.4 V is lower for the TDF8599A than for the other two amplifiers. It is therefore advised to use the TDF8597 or the TDF8599B for applications having supply voltages of up to 24 V.

1.4 Block diagram

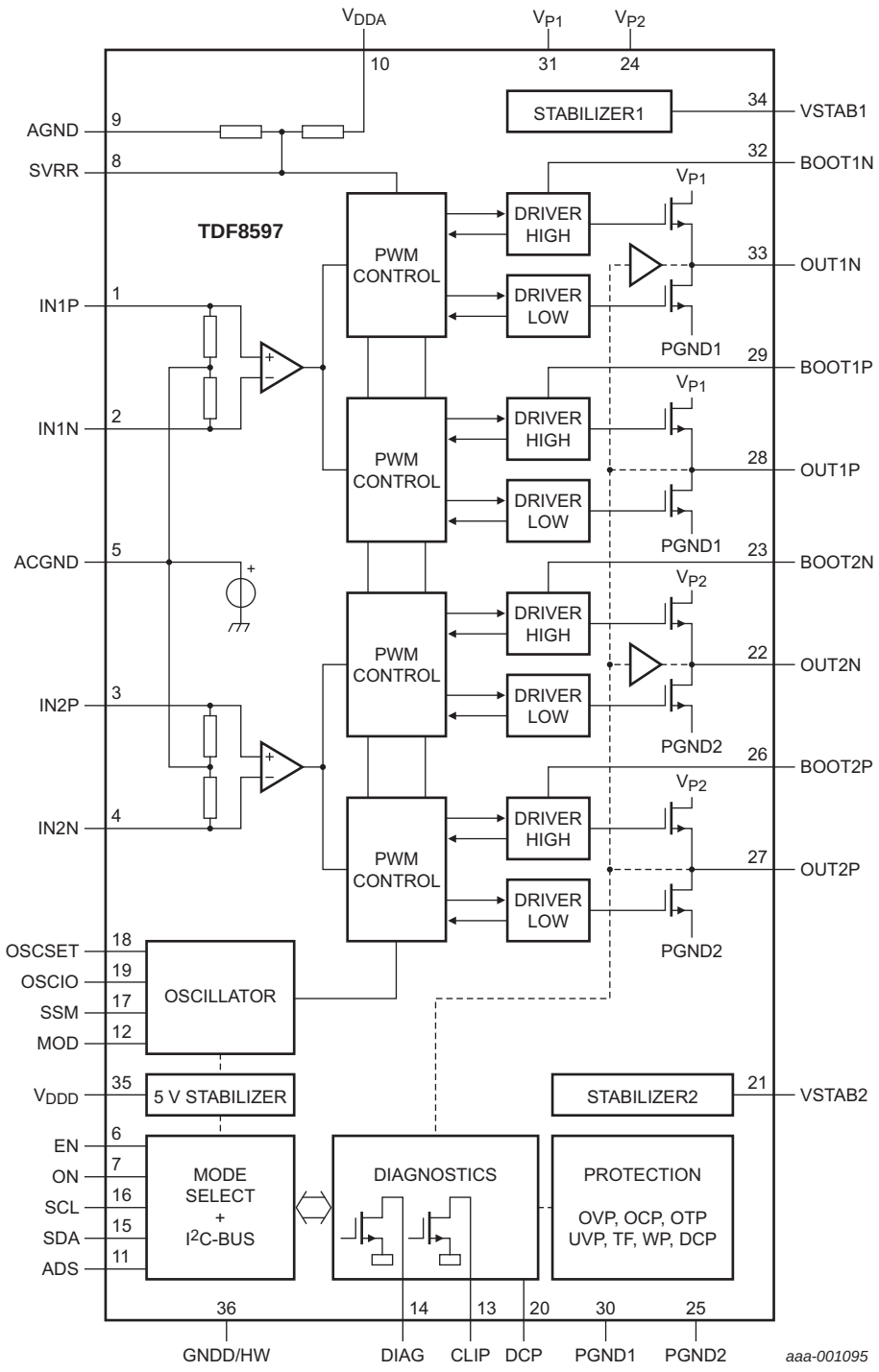


Fig 1. Block diagram of the TDF8597 (TDF8599A and TDF8599B are similar)

1.5 Pinning information

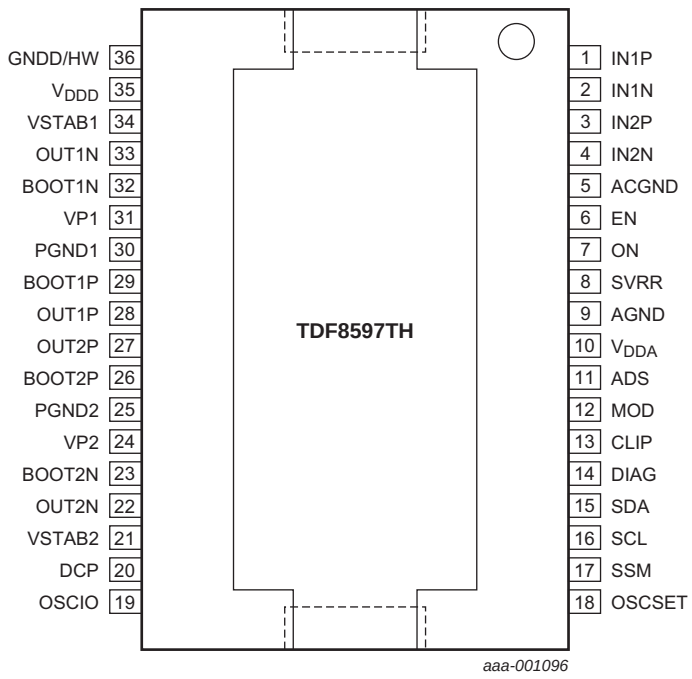


Fig 2. Heatsink up (top view) pin configuration TDF8597TH package HSOP36 (TDF8599B and TDF8599A are identical)

1.5.1 Pin description

Table 5. Pin description for the TDF8597, TDF8599A and TDF8599B

Symbol	Pin	Type[1]	Description
IN1P	1	I	channel 1 positive audio input
IN1N	2	I	channel 1 negative audio input
IN2P	3	I	channel 2 positive audio input
IN2N	4	I	channel 2 negative audio input
ACGND	5	I	decoupling for input reference voltage
EN	6	I	enable input: non-I^{2}C-bus mode: switch between off and Mute mode I^{2}C-bus mode: off and Standby mode
ON	7	I	switch between Mute mode and On
SVRR	8	-	decoupling for internal half supply reference voltage
AGND	9	G	analog supply ground
V_{DDA}	10	P	analog supply voltage [2]
ADS	11	I	non-I^{2}C-bus mode: connected to ground I^{2}C-bus mode: address selection pin
MOD	12	I	modulation mode and phase shift select
CLIP	13	O	open-drain clip output
DIAG	14	O	diagnostic output; open-drain
SDA	15	I/O	I^{2}C-bus data input and output

Table 5. Pin description for the TDF8597, TDF8599A and TDF8599B *...continued*

Symbol	Pin	Type[1]	Description
SCL	16	I	I^2C-bus clock input
SSM	17	-	master setting: Spread spectrum mode frequency slave setting: phase lock operation
OSCSET	18	-	master/slave oscillator setting master only setting: set internal oscillator frequency
OSCIO	19	I/O	slave setting: external oscillator input master setting: internal oscillator output
DCP	20	I	DC protection input for the filtered output voltages
VSTAB2	21	-	decoupling internal stabilizer 2 for DMOST drivers
OUT2N	22	O	channel 2 negative PWM output
BOOT2N	23	-	bootstrap capacitor for channel 2 negative
V_{P2}	24	P	channel 2 power supply voltage [2]
PGND2	25	G	channel 2 power ground
BOOT2P	26	-	bootstrap capacitor for channel 2 positive
OUT2P	27	O	channel 2 positive PWM output
OUT1P	28	O	channel 1 positive PWM output
BOOT1P	29	-	bootstrap capacitor for channel 1 positive
PGND1	30	G	channel 1 power ground
V_{P1}	31	P	channel 1 power supply voltage [2]
BOOT1N	32	-	bootstrap capacitor for channel 1 negative
OUT1N	33	O	channel 1 negative PWM output
VSTAB1	34	-	decoupling internal stabilizer 1 for DMOST drivers
V_{DDD}	35	-	decoupling of the internal 5 V logic supply
GNDD/HW	36	G	ground digital supply voltage and handle wafer connection

[1] I = input, O = output, I/O = input/output, G = ground and P = power supply.

[2] In this data sheet, supply voltages V_{P1}, V_{P2} and V_{DDA} is referred to as V_P.

2. Application circuit

2.1 Introduction

Class-D amplifiers are switching devices which operate at relatively high frequencies, similar to switch-mode power supplies. Due to the switching characteristics, the PCB lay-out and the choice of components have great influence on the EMI behavior of the amplifier. In order to comply with the strict EMI standards used in the automotive industry, a good PCB design is vital. In this section, the application PCB which is available at this moment is described. The PCB design considerations are elaborated and the schematics and lay-out are shown.

2.2 Basic PCB design rules

Basic rules for a good PCB design for a class-D amplifier are:

- Keep loops as small as possible

- Place bootstrap capacitors as close as possible to the IC pins
- Place decoupling components as close as possible to the IC pins (to reduce loops)
- Use ferrite inductors in the supply lines (not in the output lines)
- Use a solid ground plane to reduce resistance and loop surface
- Place resonance damping circuits (snubbers) at the outputs, preferably as close as possible to the IC pins
- Electrically isolate the heat sink from the device
- Preferably, place all connectors on one side of the PCB, as close together as possible
- Connect output filter capacitors to ground as close as possible to the connector
- Use shielded filter coils, at least magnetically shielded, but additional electrical shielding may also be necessary
- PCB design must be symmetrical

2.3 Stereo application schematic

Figure 3 shows the application schematic of the TDF8597 stereo application PCB. This PCB is designed so that it can also be used for the TDF8599A and the TDF8599B.

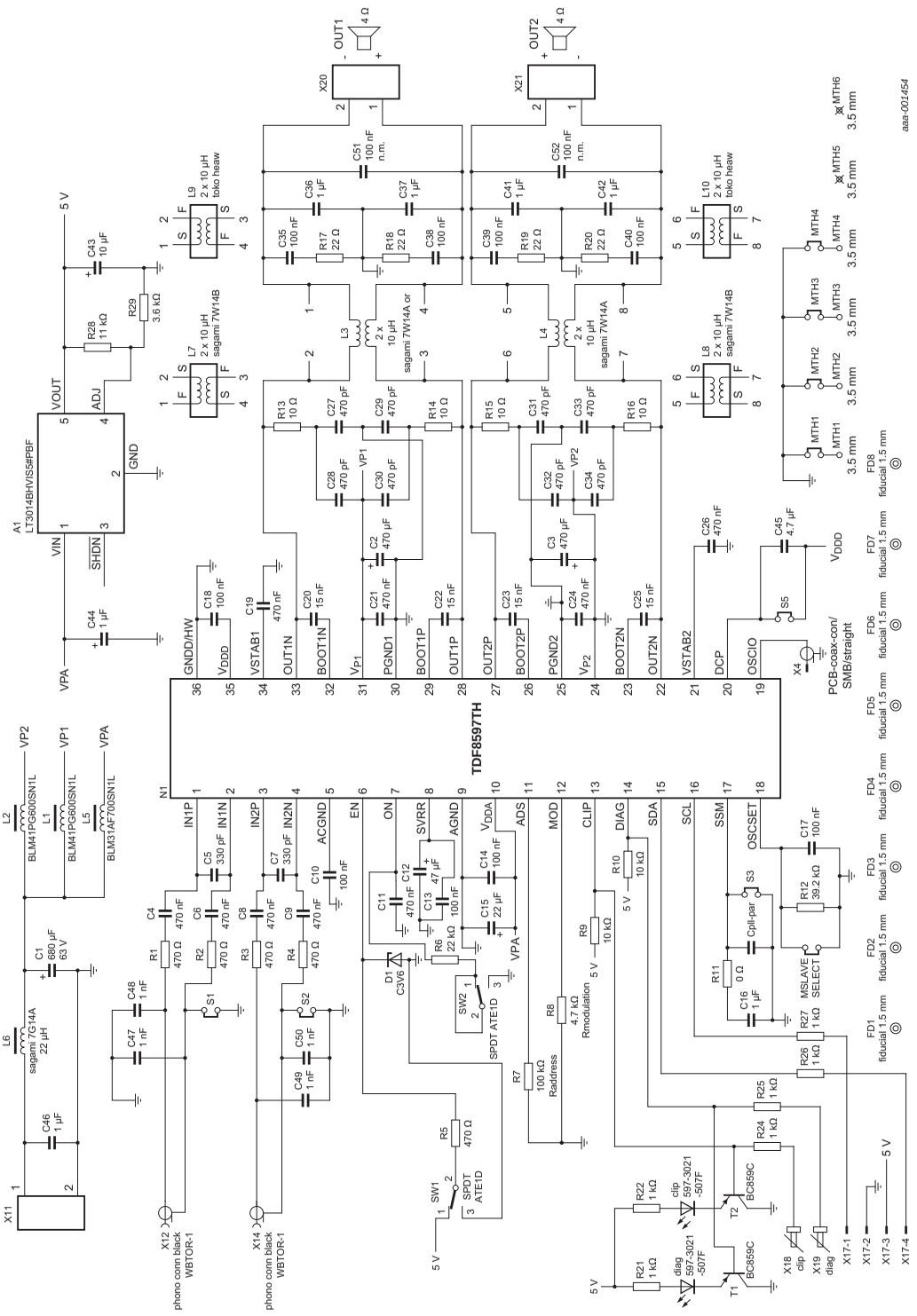


Fig 3. Application schematic for the TDF8597

2.4 Design considerations and component choices

This section explains the main schematic parts and discusses component options for each section of the schematic.

2.4.1 Power supply

Power supply decoupling is very important for good audio and EMI performance of a Class-D amplifier.

Coil L6 and capacitor C46 serve as a low-pass filter, filtering high frequency emissions from the power line. Capacitor C1 acts as a supply buffer. From C1 onwards, the power supply is separated into three circuits, V_{P1}, V_{P2} and VPA.

V_{P1} and V_{P2} are the supply circuits for the power stages; VPA is the supply for the small signal part of the amplifier.

Each power stage is HF decoupled by a ferrite bead (L1 and L2) and a 470 nF ceramic capacitor (C21 and C24). The electrolytic capacitors C2 and C3 serve a dual purpose:

- primarily they dampen any resonances from the LC combination of the beads and the ceramic capacitors
- secondly, they act as an additional supply buffer

The total ESR of the supply decoupling capacitors in the power circuit must not exceed 350 mΩ. Especially at extremely low temperatures, the ESR of electrolytic capacitors increases. If the ESR exceeds 350 mΩ, oscillations can occur just after the amplifier is switched on. These oscillations increase the supply current. Oscillations can be prevented by using capacitors which have a sufficiently low ESR at the required minimum operating temperatures.

The supply for the small signal part (pin 10, V_{DDA}) is also HF decoupled by a ferrite bead (L5) and a 100 nF ceramic capacitor. Electrolytic capacitor C15 provides further supply buffering.

When the amplifier is supplied by a DC-to-DC converter which is synchronized with the amplifier oscillator, pay special attention to the decoupling of pin V_{DDA} (pin 10). If there is supply ripple at pin V_{DDA} with an amplitude above 20 mV, in phase with the oscillator frequency, it is likely that the internal circuit, which determines the switch-on timing, cannot enable the output stages, or delays switch-on for a long period. Pay special attention to the ferrite bead used for decoupling pin V_{DDA}. Choose a bead resistance that will not cause a resonance at the oscillator frequency. At supply voltages of 24 V and above (TDF8599A), a 4.7 Ω resistor can be used instead of the ferrite bead.

2.4.2 Output filtering

Since the unfiltered output signal of a class-D amplifier is a pulse-width modulated square wave signal with a frequency of 300 kHz or higher, any artifacts, such as overshoot or ringing at the outputs, results in high frequency interference. The design of the output stage and its filtering is therefore vital to the EMI performance of the amplifier.

Small RC filters (snubbers: R13, R14, R15, R16, C27 to C30 and C31 to C34) are placed as close as possible to the output pins. These filters are necessary to dampen any overshoot at the outputs. The output signal is low-pass filtered by the LC combination of

the 10 μH coils and the 1 μF capacitors (L3 and L4 and C36, C37, C41 and C42). Optimum component values for second-order Butterworth filters with a cut-off frequency of approximately 45 kHz are given in Table 6.

Table 6. Butterworth filter component values for each channel

Modulation:	AD	BD	AD	BD	AD	BD
R_L:	4 Ω		2 Ω		1 Ω	
L:	2 × 10 μH	2 × 10 μH	2 × 5 μH	2 × 5 μH	2 × 2.5 μH	2 × 2.5 μH
C:	470 nF	2 × 1 μF	1 μF	2 × 2.2 μF	2.2 μF	2 × 4.7 μH

The coils must be magnetically shielded and have excellent linearity in the audio frequency range. Ensure that the coil saturation current in all the coils corresponds to the maximum output current (8 A) of the amplifier. If a short-circuit occurs at one of the outputs or across the outputs, the output current can rise above 8 A (up to 11 A per output). In such a case, there is a risk of damage to the output stages if the inductance value of the output filter coils is less than L_{min} given in Table 7.

The minimum inductance value (L_{min}) of the output coils, required to prevent damage to the output stages, depends on the supply voltage in stereo mode and parallel mode, and is shown in Table 7.

Table 7. Minimum inductance of output coils in a short-circuit

Parameter	TDF8597/TDF8599B				TDF8599A	
	Stereo		Parallel		Stereo	Parallel
Maximum peak output current	20 A		26 A		18 A	25 A
Overcurrent protection output current ($I_{O(ocp)}$)	11 A		22 A		11 A	22 A
Supply voltage (V_P)	18 V	24 V	18 V	24 V	35 V	35 V
Minimum inductance (L_{min})	260 nH	347 nH	585 nH	780 nH	650 nH	1.5 μH

If the value of L_{min} cannot be guaranteed, take additional measures at the output stages to prevent their damage if a short-circuit occurs.

It is recommended that film capacitors are used for the filter capacitors for the best audio performance. When ceramic (SMD) capacitors are used, ensure that at least X7R material is used. The DC breakdown voltage of these capacitors must be at least 50 V to prevent damage to them from any voltage spikes at the outputs.

It is vital that the filter capacitors are grounded as close as possible to the supply ground connection, for good EMI performance.

In addition to the LC filter, two small RC filters (R17 to R20, C35 and C38 to C40) are added to act as resonance dampers in case no load is connected to the output. If the load is disconnected and the signal frequency approaches the filter resonance frequency, these resonance dampers protect the output stage. In such cases, the output current can increase dramatically, possibly damaging the output stage.

2.4.3 Bootstrap capacitors

The bootstrap capacitors (C20, C22, C23 and C25) provide the drive current for the output transistors. Place them as close as possible to the device pins.

2.4.4 VSTAB capacitors

The VSTAB capacitors C19 and C26 act as decoupling capacitors for the internal voltage stabilizers VSTAB1 and VSTAB2. These capacitors must also provide the drive current for the bootstrap capacitors. To ensure a sufficient drive current for the bootstrap capacitors, the value of these capacitors must always be 220 nF or higher. Connect the capacitors to ground as close as possible to the supply ground pins.

2.4.5 Input circuit

The main components of the input circuit are the 470 nF (C4, C6, C8, C9) decoupling capacitors. The 4.7 kΩ resistors (R1 to R4), 1 nF capacitors (C47 to C50) and 330 nF capacitors (C5, C7) are all used for filtering unwanted high frequency disturbance.

The TDF8597, TDF8599A and TDF8599B have symmetrical (balanced) inputs. If an unbalanced (single-ended) signal source is used, the negative inputs can be AC-connected to ground. For the best possible performance, it is important to connect the ground in front of the input resistors to ensure that the input circuit stays symmetrical.

A small DC leakage current at the inputs can cause a relatively high DC shift at the output, so it is important that the input capacitors have a low DC leakage current. Use film capacitors for optimum sound quality, otherwise use good quality ceramic capacitors (X7R or NPO material).

2.4.6 SVR capacitor

In addition to stabilizing the internal voltage reference for the input circuits, the SVR capacitor also acts as a timing element for the switch-on sequence of the amplifier. Reducing the value of the SVR capacitor reduces the switch-on time of the amplifier, which can result in audible switch-on pops.

The maximum voltage on pin SVR is half the supply voltage, so the voltage rating of the SVR capacitor can be chosen accordingly.

2.4.7 DCP capacitor

The DCP capacitor (C45) determines the cut-off frequency for the DC-offset protection circuit. The 4.7 μF capacitor ensures proper operation of this circuit down to frequencies of 20 Hz. If the amplifier is used as a subwoofer amplifier, it may be advisable to increase the value of this capacitor to 10 μF or even 22 μF. The leakage current of this capacitor must not exceed 3 μA. Connect the second terminal of the capacitor to V_{DDD} (Pin 35).

2.4.8 Pin ON capacitor

The capacitor at pin ON (C11) acts as a timing element for the DC-load detection test and determines the transition time between the mute and the operating condition

2.5 Stereo application BOM list

2.5.1 Capacitors

Table 8. Capacitors used in the standard application PCB

Quantity	Reference	Part	Manufacturer	Type
1	C1	680 μF/63 V	Panasonic	EEUFC1J681
2	C2, C3	470 μF/35 V	Nichicon	UPS1V471MPD
4	C4, C6, C8, C9	470 nF/16 V SMD film	Panasonic	ECPU1C474MA5
2	C5, C7	330 pF/50 V SMD 0603 COG	non-specific	-
9	C10, C13, C14, C17, C18, C35, C38, C39, C40	100 nF/50 V SMD 0805 X7R	non-specific	-
1	C11	470 nF/16 V SMD 0805 X7R	non-specific	-
1	C12	47 μF/25 V	Rubycon	35ZLJ47M5X11
1	C15	22 μF/35 V	Multicomp	MCRH35V226M5X11
2	C16, C46	1 μF/50 V SMD 1206 Y5V	non-specific	-
4	C36, C37, C41, C42	1 μF/63 V MKT	Epcos	B32529C105K
2	C19, C46	220 nF/50 V SMD 0805 X7R	non-specific	-
8	C20, C22, C23, C25	15 nF/50 V SMD 0603 COG	non-specific	-
2	C21, C24	470 nF/50 V SMD 0805 X7R	AVX	0805C474KAZ2A
8	C27, C28, C29, C30, C31, C32, C33, C34	470 pF/50 V SMD 0603 COG	non-specific	-
1	C45	4 μ7/16 V SMD 1206 Y5V	non-specific	-
1	C44	1 μF/50 V Elcap	non-specific	
1	C43	10 μF/35 V Elcap	non-specific	
4	C47, C48, C49, C50	1 nF/50 V SMD 0603 COG	non-specific	

2.5.2 Resistors

Table 9. Resistors used in the standard application PCB

Quantity	Reference	Part	Manufacturer	Type
4	R1, R2, R3, R4	4.7 kΩ/0.1 W SMD 0805	non-specific	-
1	R5	470 Ω/0.1 W SMD 0805	non-specific	-
2	R6, R23	22 kΩ/0.1 W SMD 0805	non-specific	-
1	R7	R address, 100 kΩ/0.1 W/1 % SMD 0805	non-specific	-
1	R7	R modulation, 4.7 kΩ/0.1 W SMD 0805	non-specific	-
2	R9, R10	10 kΩ/0.1 W SMD 0805	non-specific	-
1	R11	0 Ω SMD 0805	non-specific	-
1	R12	39 kΩ/0.1 W SMD 0805	non-specific	-
4	R13, R14, R15, R16	10 Ω/0.25 W SMD 1206	non-specific	-
4	R17, R18, R19, R20	22 Ω/0.25 W SMD 1206	non-specific	-
6	R21, R22, R24, R25, R26, R27	1 kΩ/0.1 W SMD 0805	non-specific	-

2.5.3 Semiconductors

Table 10. Semiconductors used in the standard application PCB

Quantity	Reference	Part	Manufacturer	Type
1	U1	TDF8597TH	NXP Semiconductors	TDF8597TH, TDF8599BTH, TDF8599ATH
1	A1	stabi	National Semiconductors	LT3014BHVIS5#PBF
2	T1, T2	BC859	NXP Semiconductors	BC859
2	Diag, Clip	SMD LED	Dialight	597-3021-507F
1	D1	3V6 Zener diode	NXP Semiconductors	BZX79-C3V6

2.5.4 Inductors

Table 11. Inductors used in the standard application PCB

Quantity	Reference	Part	Manufacturer	Type
2	L1, L2	ferrite bead	Murata	BLM41PG600SN1L
2	L3, L4	filter coil	Toko or Sagami	HEAW 10 μH, 7W14A 10 μH, 7W14B 10 μH, DBE1010HB 10 μH
1	L5	ferrite bead	Murata	BLM31AF700SN1L
1	L6	supply coil	Sagami	7G14A 22 μH

Components that do not specify manufacturer and type number do not require a specific manufacturer if they fulfill the requirements for size, material, breakdown voltage and power rating.

Since the PCB is designed to accommodate the TDF8597TH, TDF8599BTH and the TDF8599ATH, the components have been selected to operate properly up to the highest expected supply voltage (35 V for the TDF8599A). When a PCB is designed that is not expected to operate at these supply voltages, components with a lower breakdown can also be used. It is always advisable to use components with a sufficient margin in their maximum breakdown voltage, especially for the HF decoupling capacitors in the supply lines.

2.5.5 Stereo application PCB layout

The TDF8597TH (and TDF8599ATH and TDF8599BTH) application PCB has two layers. The PCB has been designed mainly for audio evaluation purposes. For EMI testing, the PCB is required to be mounted either in a car radio-like box or on a flat aluminum plate.

Although it is advised to locate all connectors on one side of the PCB, in this PCB the input connectors have been placed at the side of the PCB for easier access. Since the inputs are grounded through the general ground plane, there is no issue of increased EMI as a result of large differences in ground levels.

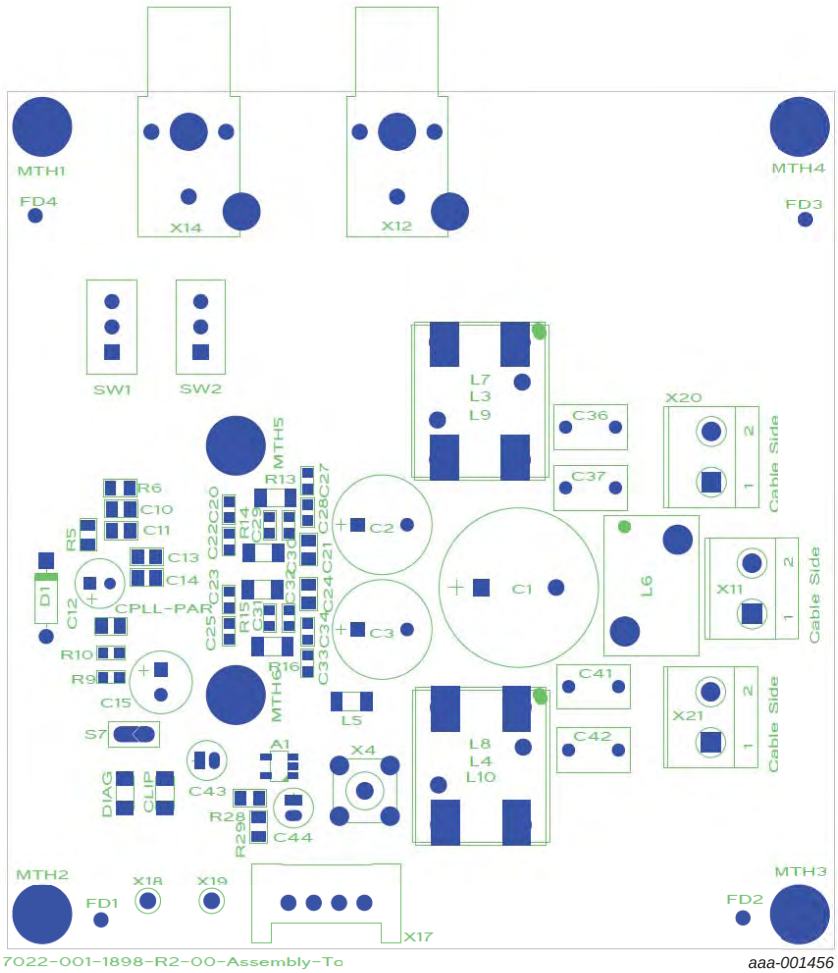


Fig 4. Top assembly view of the application PCB

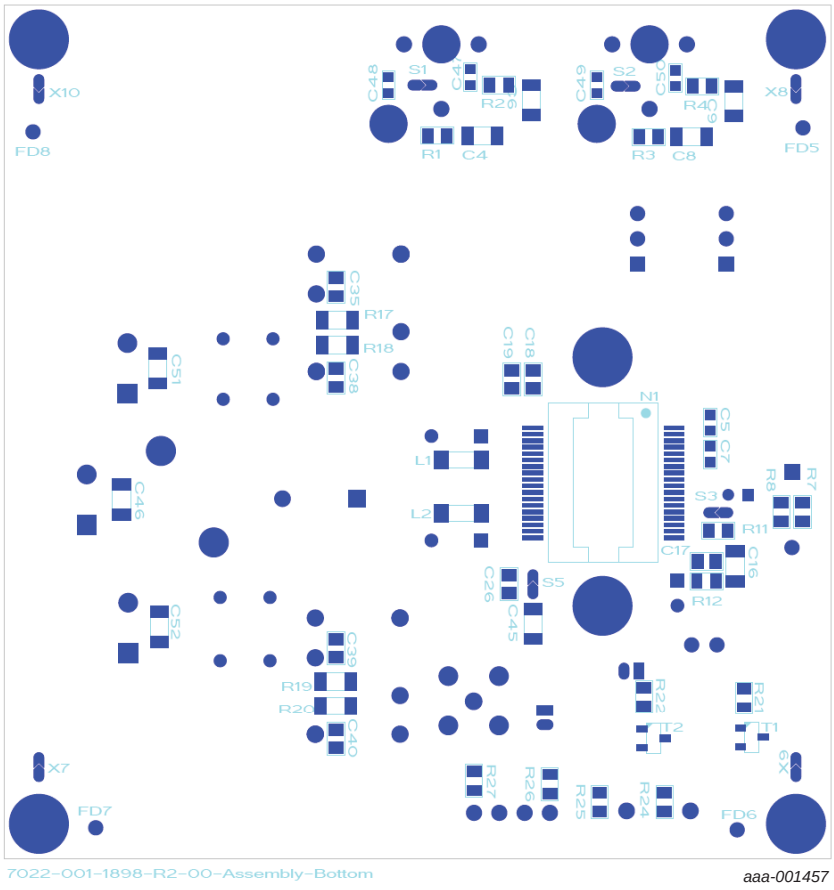
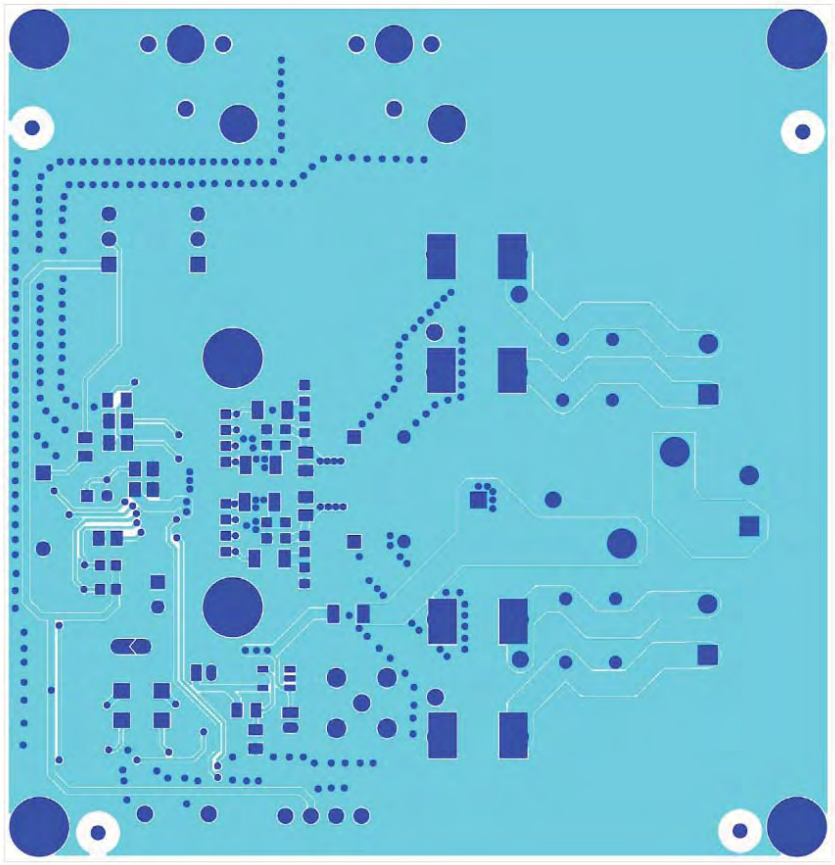
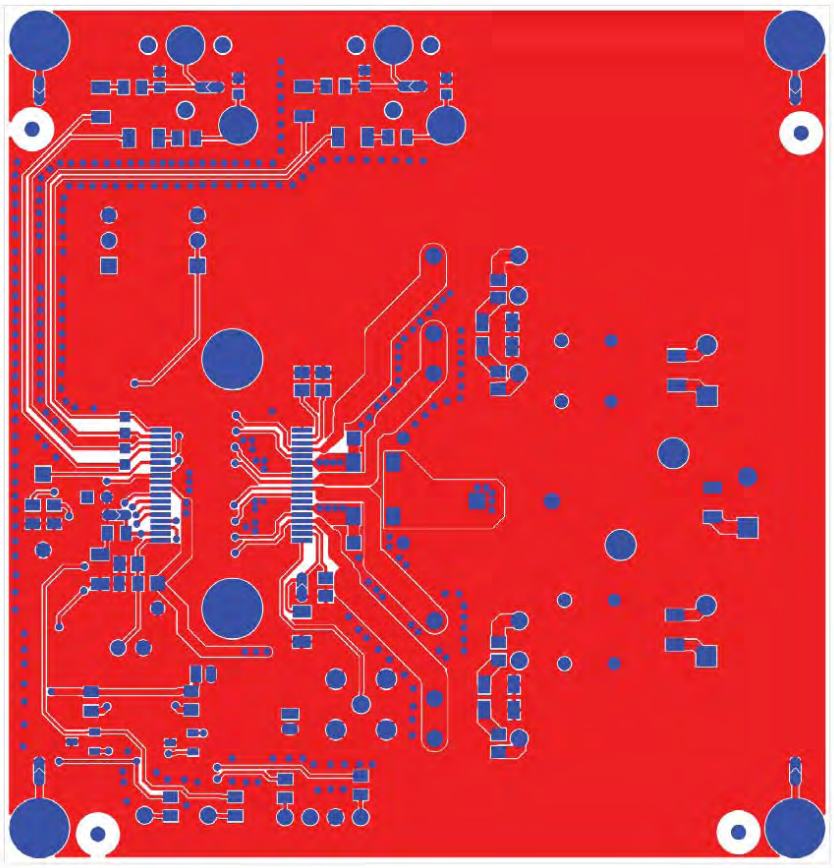


Fig 5. Bottom assembly view of the application PCB



aaa-001458

Fig 6. Top copper layer



aaa-001460

Fig 7. Bottom copper layer

3. Operating modes

3.1 AD modulation versus BD modulation

The TDF8597, TDF8599A and TDF8599B can be used in AD modulation mode or in BD modulation mode. In I^2C operation, the modulation mode is determined through I^2C control. In the Legacy mode, the modulation mode can be determined using the resistor at pin MOD (pin 12).

The advantages of BD modulation are:

- Lower output noise level
- Lower THD and noise
- Lower switch-on pop
- Better channel separation
- Better SVRR

A disadvantage of BD modulation is that it requires larger value filter capacitors connected to ground than when the device is being used in AD modulation.

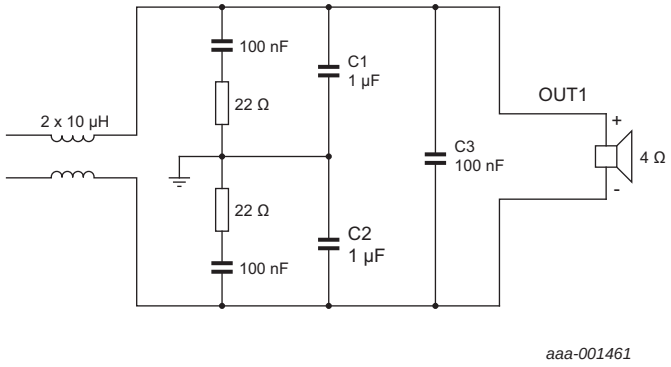


Fig 8. Filter schematic for BD modulation

The filter for BD modulation needs two 1 µF capacitors (C1 and C2), preferably film capacitors (for optimum sound quality). The 100 nF capacitor across the load (C3) can be a ceramic capacitor (X7R dielectric or better). The two RC filters (100 nF, 22 Ω) are needed for damping resonances in case the load is disconnected.

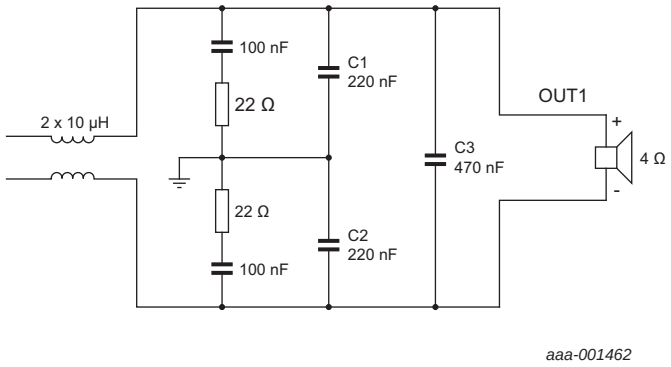


Fig 9. Filter schematic for AD modulation

Although the AD filter schematic is similar, only one 470 nF (preferably film) capacitor (C3) and two ceramic (X7R) 220 nF capacitors (C1 and C2) are required. The total cost of this second filter is lower than the BD filter.

The filter which is optimized for BD modulation can be used for an amplifier in AD modulation mode without problems. The AD modulation filter cannot be used for amplifiers in BD modulation mode.

3.2 Parallel output mode

The TDF8597, TDF8599A or TDF8599B can be set in parallel output mode using the resistor connected to pin MOD.

If the amplifier is set to parallel mode, it changes from a stereo amplifier to a mono amplifier, capable of delivering twice the current of one channel. The TDF8599B and the TDF8597 are then able to drive a 1 Ω load and the TDF8599A is able to drive a 2 Ω load.

In this mode, connect both outputs of each channel together internally and the inputs in anti-phase as shown in Figure 10.

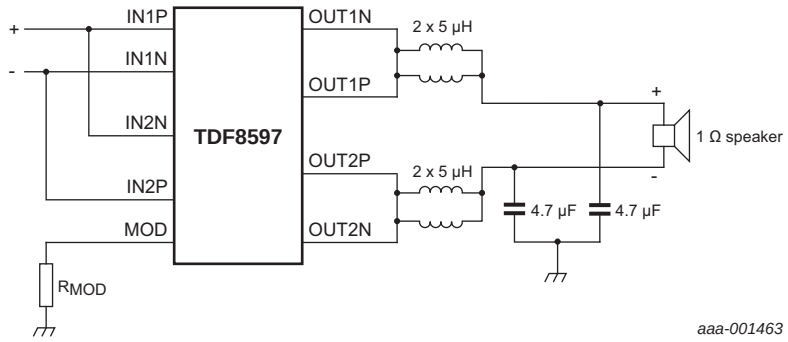


Fig 10. Parallel mode with outputs connected internally

If the two outputs are paralleled as described, the diagnostics automatically adapt to the mode of operation.

If the amplifier is used in parallel mode, it is preferable for the output pins to be connected together as close as possible to the device. If the 2 Ω filters are still in place, connect both sides of the coils together as shown in Figure 10.

Figure 11 shows the most preferred filter configuration for 1 Ω parallel operation.

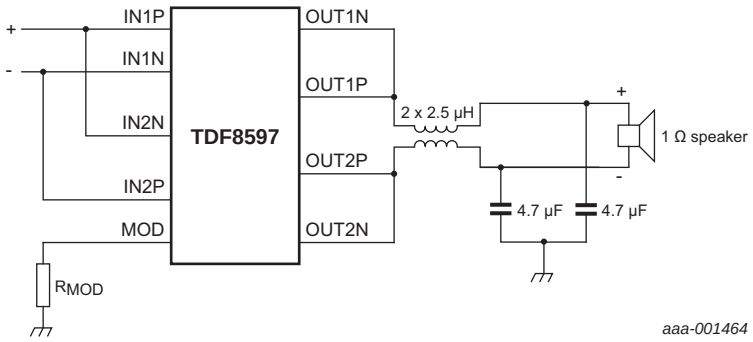


Fig 11. Parallel mode with outputs connected internally (preferred filter configuration)

Using a single coil per output minimizes the risk of resonances occurring in the filters, which can influence the THD performance.

The recommended filter components for the TDF8599A in parallel mode (2 Ω load) are: 5 µH coils and 2.2 µF filter capacitors.

3.3 Master and slave modes

In a system where multiple amplifiers are used together, the oscillators of the different devices can be synchronized. In such a system, one device can be used as master. Its oscillator frequency is determined by the resistor connected to pin OSCSET (pin 18). The other devices can then be set as slave devices by connecting pin OSCSET to ground.

When a device is used in slave mode, jitter of the external oscillator signal can be reduced by setting the device in the phase lock mode. Phase lock operation is also required to enable phase staggering. Phase lock operation is enabled with the oscillator in Slave mode and connecting a network of two capacitors C_{PLL_S} and C_{PLL_P} and resistor R_{PLL} between pin SSM and AGND. See figure 12. Connecting pin SSM directly to AGND disables this Phase lock operation causing the slave to use the external oscillator signal directly.

The values for C_{PLL_S}, C_{PLL_P} and R_{PLL} depend on the desired loop bandwidth B_{PLL} of the PLL. R_{PLL} is given by Equation 1.

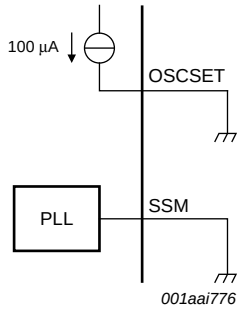
$$R_{PLL} = 8.4 \times B_{PLL}[\Omega] \quad (1)$$

The corresponding values for C_{PLL_S} and C_{PLL_P} are given by Equation 2 and Equation 3.

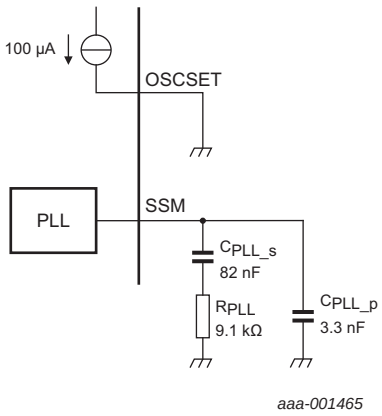
$$C_{PLL\_S} = \frac{0.8}{R_{PLL} \times B_{PLL}} \quad (2)$$

$$C_{PLL\_P} = \frac{0.032}{R_{PLL} \times B_{PLL}} \quad (3)$$

If the OSCIO input is connected to a clock master with spread spectrum mode enabled, the PLL loop bandwidth B_{PLL} should be $100 \times f_{SSM}$. Experiments have shown that a good loop bandwidth for the PLL is 1 kHz.



a. Off



b. On

Fig 12. Phase lock operation

Several tests of the TDF8597, TDF8599A and TDF8599B have shown that good values for R_{PLL}, C_{PLL_S} and C_{PLL_P} are 9.1 kΩ, 82 nF and 3.3 nF.

When a slave device is used in PLL mode, it is important that the PLL is locked before the outputs of the slave device start switching. When the channels start switching while the PLL is not yet locked, a switch-on pop can occur.

If the external oscillator signal level reduces, the phase-lock circuit can lose regulation. In such cases there is a risk that the oscillating frequency at the amplifier outputs reduces to a value close to the resonance frequency of the output filter, damaging the outputs in extreme cases. This is effectively prevented by clamping pin SSM to pin V_{DDD} (pin 35)

with a diode. With this diode in place, the slave amplifier continues to switch at a frequency of approximately 200 kHz even when the external oscillator signal is removed.

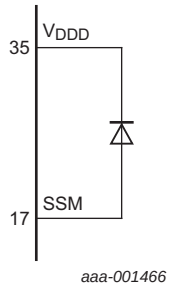


Fig 13. Clamping pin SSM to V_{DDD} with a diode

If two stereo amplifiers (such as the TDF8597 or the TDF8599B and a TDF8597 or TDF8599A) are used in a master/slave configuration, both amplifiers can run at the same oscillator frequency (the single PCM frequency). However, if combining the TDF8530 (the 4-channel device similar to the TDF8597) and a TDF8597 or TDF8599A/B in a master/slave configuration, pay special attention to the configuration setup. Normally, the oscillator frequency of the TDF8530 is twice the PWM frequency, whereas the oscillator frequency of the TDF8597 and the TDF8599A/B matches the PWM frequency. Using the TDF8530 as a master device results in the TDF8597 or TDF8599A/B running at twice the optimum clock frequency. This can be solved in several ways:

- Use the TDF8530 as the master device, but set its oscillator frequency to match the single PWM frequency by setting IB3[D2] to logic 0. The output signal at pin OSCIO is then the single PWM frequency. It is advisable to use the slave devices in PLL mode to compensate for any disturbances to the clock signal. This configuration is shown in Figure 14.
- Use the TDF8597 or TDF8599A/B as the master device and the TDF8530 as the slave device. In this case, set the TDF8530, IB3[D2] to logic 0 so that the TDF8530 is set to accept the single PWM frequency at pin OSCIO. Also set the TDF8530 to PLL mode for optimum performance as shown in Figure 15.

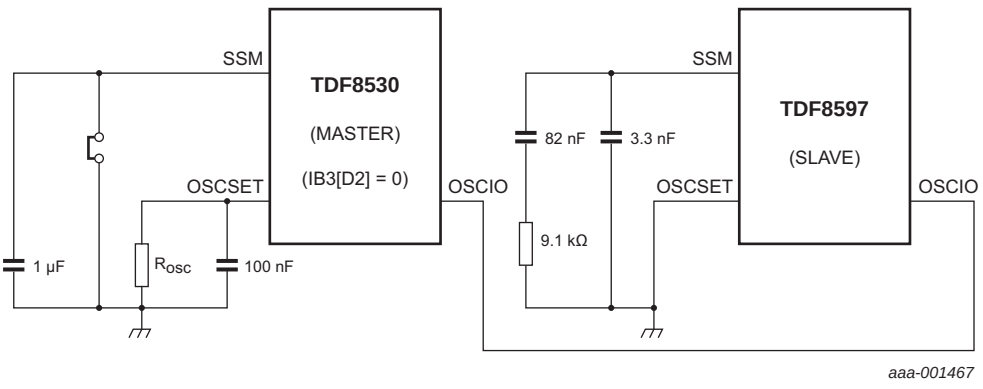


Fig 14. Master-slave combination with TDF8530 as master

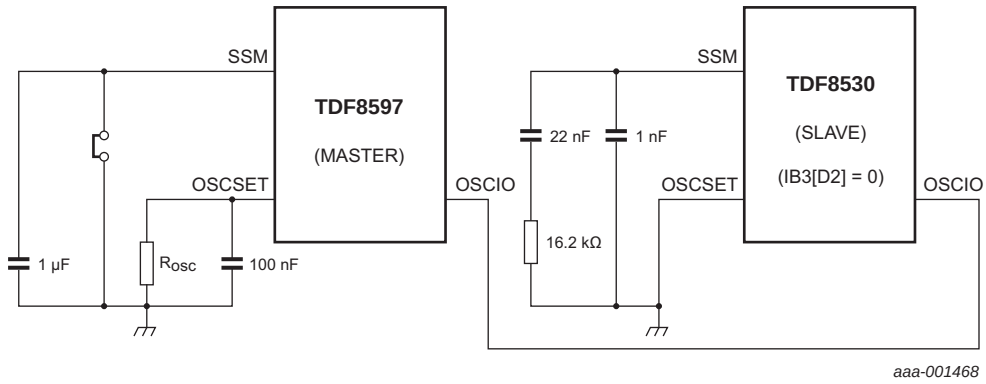


Fig 15. Master-slave combination with TDF8597 as master

If the TDF8530 is set to PLL mode when IB3[D2] = 0, it internally multiplies the external clock signal by 2, so that its clock runs at twice the PWM frequency, enabling it to use phase staggering between channels 1 and 2 and channels 3 and 4.

3.4 I²C mode and legacy mode

The TDF8597, TDF8599A and TDF8599B can either be used in legacy mode or in I²C control mode. The device can be set to legacy operation by connecting pin ADS (pin 11) to ground. In legacy mode, the diagnostics are limited to pin DIAG and pin CLIP. Modulation mode can be adjusted with a resistor connected to pin MOD (pin 12).

In I²C mode, the diagnostics are more elaborate and settings can be adjusted with I²C commands.

3.5 I²C address selection

Define the TDF8597 I²C address using specific resistor values at pins ADS and MOD. The resistor values required to set different I²C addresses are shown in Table 12.

Table 12. I²C-bus write address selection for the TDF8597

R_{ADS} (kΩ)	Stereo mode		Parallel mode	
	R_{MOD} (kΩ)			
	0[1]	6.8	33	100
100	54h	64h	54h	64h
33	52h	62h	52h	62h
6.8	50h	60h	50h	60h
0[1]	non-I²C-bus mode			

[1] Short-circuit to ground.

As an example, if pin ADS is connected to ground by R_{ADS} with a value of 100 kΩ and pin MOD is connected to ground by R_{MOD} = 6.8 kΩ, the I²C write address of the amplifier is 64h and the amplifier is set in stereo mode.

The TDF8599A and TDF8599B have 15 user-definable I²C addresses selectable by connecting resistors from pins ADS and MOD to ground. The resistor values required to set different I²C addresses for the TDF8599A and TDF8599B are shown in Table 13.

Table 13. I²C-bus write address selection for the TDF8599A and TDF8599B

R_{ADS} (kΩ)	Stereo mode			Parallel mode		
	R_{MOD} (kΩ)					
	0[1]	4.7	13	33	100	Open
Open	58h	68h	78h	58h	68h	78h
100	56h	66h	76h	56h	66h	76h
33	54h	64h	74h	54h	64h	74h
13	52h	62h	72h	52h	62h	72h
4.7	50h	60h	70h	50h	60h	70h
0[1]	non-I²C-bus mode					

[1] Short-circuit to ground.

As an example, if TDF8599A pin ADS is connected to ground by R_{ADS} = 33 kΩ and pin MOD is connected to ground by R_{MOD} = 4.7 kΩ, the I²C write address of the amplifier is 64h and the amplifier is set in stereo mode.

3.6 I²C control software for the TDF8599A and TDF8599B

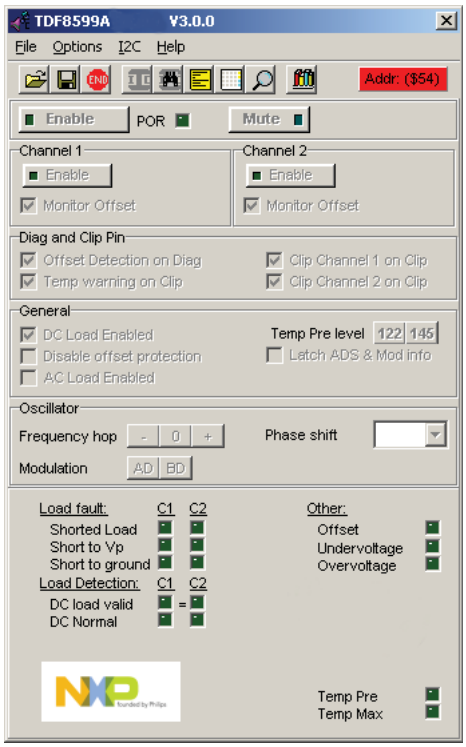
NXP Semiconductors provides customers with I²C control software to enable customers to use I²C to control the amplifier. Install the software on a PC or laptop, and connect an I²C interface (USM or UDM) to one of the computer's USB outputs to interface the computer and the amplifier.

3.6.1 Installation

Install the I²C software by double-clicking on the file TDF8599_3_.exe (for the TDF8599A and the TDF8599B). The interface software and USB drivers are then installed automatically.

3.6.2 Operation

When the software is installed, connect the interface to a USB connector on the computer. When the software starts, a control screen appears as shown in Figure 16.

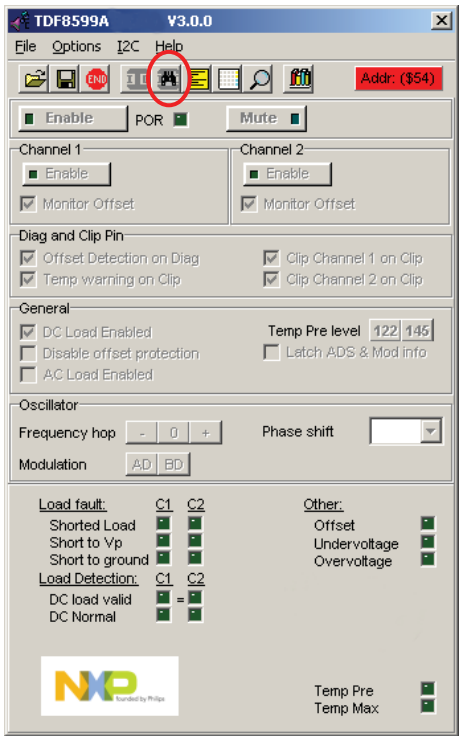


aaa-001469

Fig 16. I²C control software main screen

If the field “Addr. (XXh)” is red when a read operation is performed, there is no connection to the device. This can be caused by a wrong address setting or because the amplifier is disabled with the enable switch on the PCB. Always enable the device to allow I²C communication.

The fastest method to check that all connections are correct is by using the I²C spy function, as shown in Figure 17.



aaa-001470

Fig 17. I²C spy function

Switch on the I²C spy function by clicking the binoculars button. The screen shown in Figure 18 appears.

aaa-001471

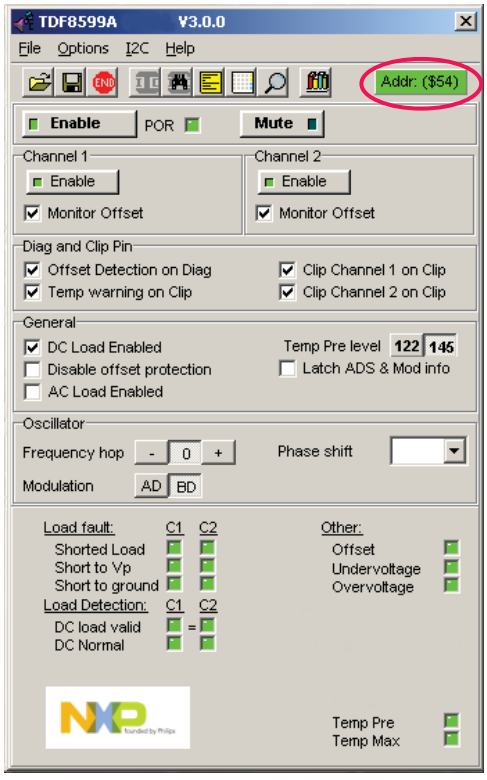
Fig 18. I²C spy screen

The software scans for connected I²C devices. When devices are found, a message appears as shown in Figure 19.

aaa-001472

Fig 19. I²C spy screen after scan is completed

The software reports which devices are found. With this information, adjust the settings to establish a connection to the amplifier. In this case, set the address to 56h. Set the address in the I²C menu. When the connection to the device is established, the Addr field turns green; see Figure 20.



aaa-001473

Fig 20. I²C screen after connection is made

The I²C control software enables control of all functions of the TDF8599ATH and TDF8599BTH with a simple user interface.

If additional direct control is needed, it is possible to switch to direct control mode enabling the direct setting of control byte bits.

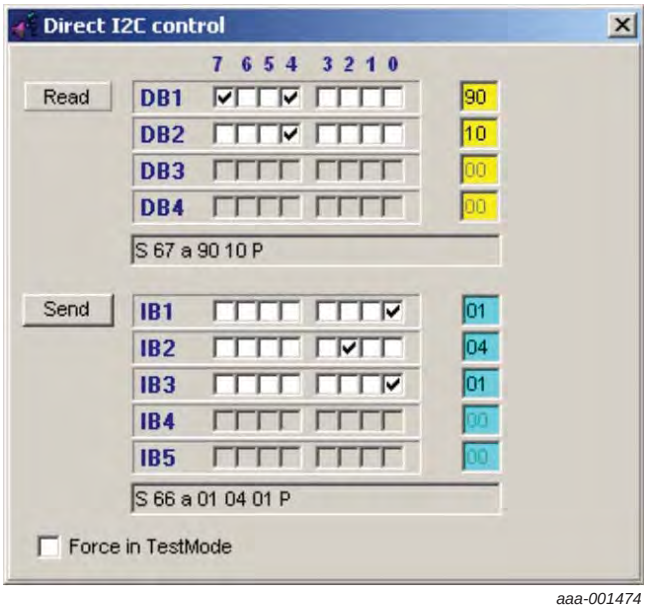


Fig 21. Direct I²C control screen

3.6.3 I²C control software for the TDF8597

Currently, there is no dedicated I²C control software available for the TDF8597. Amplifier TDF8530 is the most similar to the TDF8597, so currently, use the I²C control software that was designed for the TDF8530 to control the TDF8597. Specific TDF8597 functions which are not available in the TDF8530 software, such as selection of balanced or unbalanced inputs for 10 % clip detection, are set by bits using the direct I²C control function.

3.7 TDF8597 specific features

The TDF8597 has a number of specific features compared to the TDF8599B and the TDF8599A:

- The TDF8597 can operate at supply voltages down to 6 V, which makes it suitable for cars with start-stop functionality.
- The TDF8597 can detect a short-circuit across the load at start-up. This functionality is not available in the TDF8599A and TDF8599B, and can only be realized using a workaround as described in Section 4.2.
- The TDF8597 clip detect diagnostics can be set to 0.2 % THD (as for the TDF8599A and TDF8599B) or to 10 % THD.

The 10 % clip detection is implemented by measuring the input signal level. Since the TDF8597 inputs can be driven by either a balanced or an unbalanced input signal, it is important that the clip-detect circuit is set correctly for the input signal. This is set using the resistors connected to pins ADS and MOD.

The correct values for R_{ADS} and R_{MOD} for each mode of operation of the TDF8597 are shown in Table 14.

Table 14. R_{ADS} and R_{MOD} values for 10 % clip detection

R_{MOD} (kΩ)	Non-I²C-bus mode R_{ADS} = 0 Ω (pin ADS connected to pin AGND)		I²C-bus mode $R_{ADS} \geq$ 6.8 kΩ	
100	BD modulation	Parallel mode; no phase shift in Slave mode	Parallel mode	10 % clip detect level for symmetrically driven inputs
33	AD modulation			10 % clip detect level for asymmetrically driven inputs
6.8	BD modulation	Stereo mode; 1/2 π phase shift in Slave mode	Stereo mode	10 % clip detect level for symmetrically driven inputs
0 (short to AGND)	AD modulation			10 % clip detect level for asymmetrically driven inputs

4. Tips and hints

4.1 Diagnostics

The TDF8597, TDF8599A and TDF8599B are equipped with extensive diagnostic circuits.

At start-up, the amplifiers can detect short-circuits to ground or to the supply and if a DC-coupled load is connected. The TDF8597 can also detect a short-circuit across the load at start-up.

After start-up, a tweeter detection can be performed. During operation, the amplifier is protected against various fault conditions, such as short-circuits, output offset, and overtemperature. These fault conditions can all be read via the I²C-bus.

When the DC load diagnostic is activated via the I²C-bus, the start-up sequence is as follows:

1. The DC-load detection test is performed, enabling the amplifier to detect if a load is connected and, in the case of the TDF8597, if this load is correct or if it is a short-circuit. The diagnostic bits that are used for the DC-load detection are also used for window protection. As a result, bits DB1[D0] and DB2[D0] are set to logic 1 after the DC-load detection is performed, so that a short-circuit to ground at both outputs is indicated even if a short-circuit does not exist. After the data bits are read, bits D1[D0] and D2[D0] are reset. A second read operation gives the correct readout. Therefore, perform 2 read operations to ensure a correct readout of the load detection test and window protection test sequence.
2. After the DC-load detection has completed successfully, the amplifier checks for output short-circuits to ground or to the supply (window protection). A relatively high resistance to ground or to the supply in the output stage is recognized as a short-circuit. This avoids damage to the amplifier by preventing it being powered on during a short-circuit condition.

   Remark: A short-circuit to the supply can only be recognized as a short-circuit when the difference between the half supply voltage and the supply voltage is greater than 4 V. This may result in different diagnostic results than expected in systems where a DC-DC converter is used to increase the supply voltage of the amplifier. A short-circuit to the supply can only be detected reliably when the supply voltage of the

amplifier is equal to the battery voltage. Therefore, it is advisable to perform the DC load detection sequence while the amplifier's power supply voltage matches the battery voltage for reliable short-circuit detection at start-up.

3. If window detection has not detected a short-circuit, the amplifier is switched on and released for operation.
4. When the amplifier is fully operational, the tweeter detection test can be performed. This test requires the amplifier to be driven by an external signal. Adjust the frequency and level so that during the tweeter detection test the load current exceeds the programmed current threshold when the tweeter is connected.
5. During operation, the amplifier is protected against short-circuits by OverCurrent Protection (OCP). A short-circuit is only detected and diagnosed if the output current exceeds the OCP threshold.

4.2 Shorted load detection at start-up

Although the TDF8599A and TDF8599B are not equipped with shorted load detection at start-up, it is possible to detect a short-circuit across the load at start-up using the clip detect circuit.

Normally, a short-circuit across the load is only detected if the output current of an output stage exceeds the maximum current (8 A). To detect a short-circuit across the load requires a signal to be applied to the input, that drives the amplifier to such a level that the output current exceeds the maximum current. Detecting a shorted load is problematic at a low supply voltage due to series resistances in the circuit and the current limiting circuit preventing sufficient current being available for short-circuit detection.

The following method for detecting a short-circuit across the load uses the clip detect circuitry of the amplifier, combined with the current limiting circuit.

Applying a low frequency pulse to the amplifier input, gives a low frequency pulse at the output. Set the pulse amplitude so that the output signal is not clipped when a normal load (4 Ω or 2 Ω) is connected. If the output current does not exceed 8 A, the current limiting circuit is not activated and the amplifier output is not clipped. If the output current exceeds 8 A, the current limiting circuit activates and the output signal starts to clip. Figure 22 shows the result of connecting a 0.5 Ω load to the output causing the current limiting circuit to activate and trigger the clip-detect circuit.

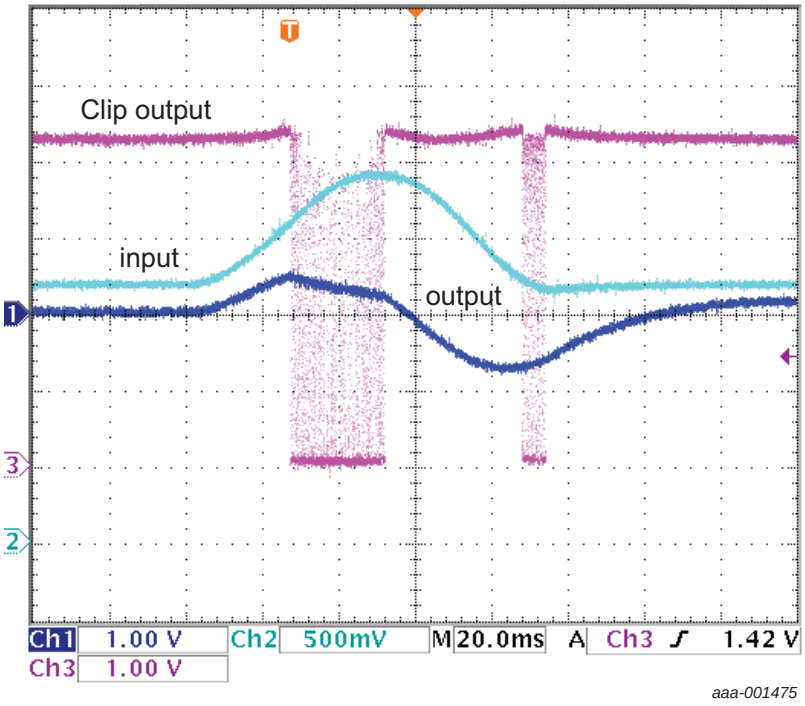


Fig 22. Shorted-load detection at start-up

The input pulse was chosen so that the shorted-load test is inaudible. The input pulse can be generated using a DSP. A custom-made solution for the DiRaNA 2 DSP is available from NXP Semiconductors.

4.3 Recommended repetitive DC-load detection procedure

If repetitive DC-load detection is required, it is advisable to activate the amplifier with both output channels disabled (IB1[D1] = 1 and IB2[D1] = 1).

If the two output channels are disabled, the DC-load detection test can be repeated by simply toggling the enable DC-load bit (IB2[D2]). This method ensures that the DC-load detection test is repeated with the least possible delay.

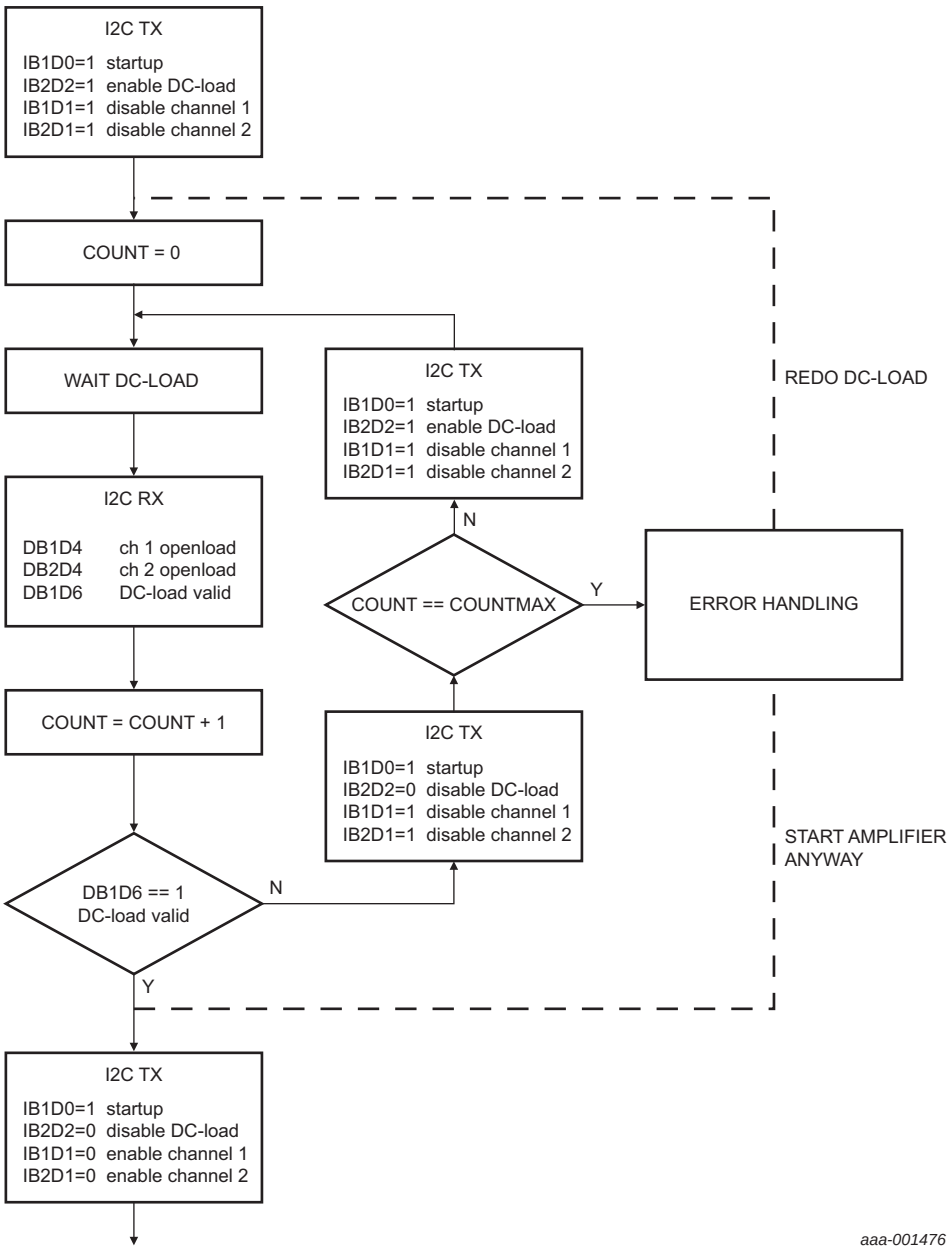


Fig 23. Recommended DC-load detection procedure

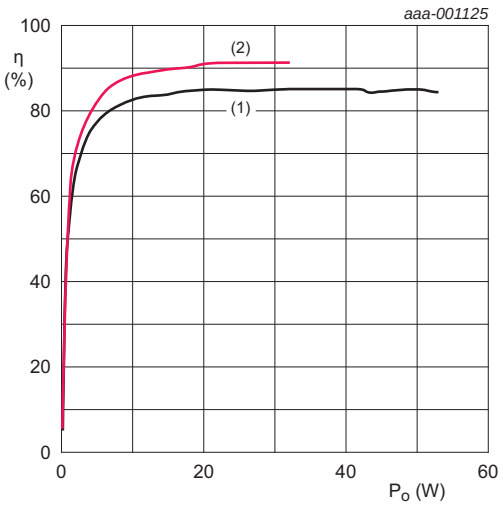
4.4 Mounting

If the amplifier is mounted on an external heatsink, electrically insulate the copper slug of the package from the external heatsink, preferably with a 1 mm thick aluminum oxide washer to limit EMI. Although the copper slug is electrically connected to the power ground of the amplifier, connecting it to the external heatsink can cause the external heatsink to act as an antenna. Using an insulating washer reduces this effect. A thick washer reduces capacitive coupling more than a thinner washer. Since aluminum oxide is an excellent conductor of heat, a thick aluminum oxide washer is the best option.

Connect the external heatsink to ground, preferably as close as possible to the power ground connection of the PCB. The maximum recommended clamping force for the HSOP36 package is 50 N.

4.5 Power dissipation and efficiency

Figure 24 shows the efficiency of the TDF8597TH at a supply voltage of 14.4 V, with 2 Ω and 4 Ω loads.

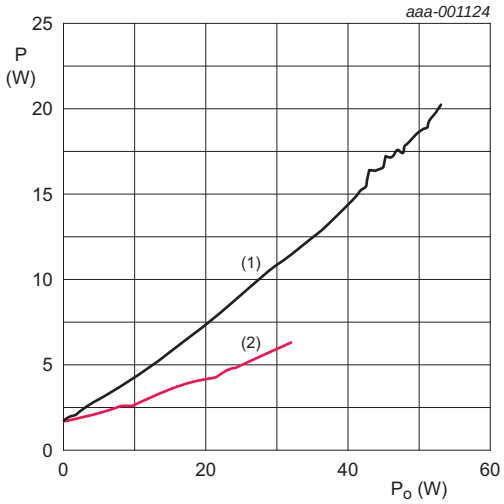


(1) R_L = 2 Ω.

(2) R_L = 4 Ω.

Fig 24. TDF8597TH efficiency as a function of P_o per channel, 2 channels driven, V_P = 14.4 V; R_L = 2 Ω and 4 Ω

Figure 24 shows that the efficiency reaches 90 % at an output power of 20 W (4 Ω load). Figure 25 shows the power dissipation of the amplifier versus the output power per channel.



(1) R_L = 2 Ω.

(2) R_L = 4 Ω.

Fig 25. TDF8597CTH power dissipation as a function of P_o per channel, 2 channels driven, V_P = 14.4 V, R_L = 2 Ω, 4 Ω

Figure 25 shows that the quiescent power dissipation of the amplifier is approximately 1.4 W.

The typical quiescent current of the device at a supply voltage of 14.4 V is 90 mA. Due to additional currents running in the output snubbers and in the output filter coils (coil losses), the total current into the application is approximately 100 mA. Since the currents caused by the snubbers and the coil losses only run through the low ohmic output transistors, these currents will not contribute to the power dissipation in the amplifier.

The coil losses and the currents in the snubbers increase if the supply voltage increases, so at 24 V (TDF8597 and TDF8599B) and at 35 V (TDF8599A) these currents add to the total quiescent current into the application.

The coil losses cause a temperature increase in the output filter coils. The choice of output filter coil type/brand can be important for the total thermal behavior of the application, particularly at high supply voltages.

4.6 Multiple devices

If more than one device is used in an application, several pins of these devices can be connected together. Pins SDA and SCL can be connected together, and pins DIAG and CLIP can be connected together. Use a diode to connect the ON pins of two devices together.

In an application where devices can be enabled and disabled individually, using pin EN, connect the oscillator pins of the devices together using 20 kΩ resistors. If the EN pins are tied together, these resistors are not required.

5. Abbreviations

Table 15. Abbreviations

Abbreviation	Description
BCDMOS	Bipolar Complementary and double Diffused Metal-Oxide Semiconductor
BTL	Bridge-Tied Load
DCP	DC-offset Protection
DMOST	double Diffused Metal-Oxide Semiconductor Transistor
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
I^2C	Inter-Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
NDMOST	N-type double Diffused Metal-Oxide Semiconductor Transistor
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse-Width Modulation
SOI	Silicon-On-Insulator
TFP	Thermal Foldback Protection
UVP	UnderVoltage Protection
WP	Window Protection

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Date of release: 18 November 2011
Document identifier: AN10741